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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,230	04/08/2004	Mark B. Fuselier	2000.092182	9406

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

MAIL DATE	DELIVERY MODE
06/03/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,230	FUSELIER ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30,56-61 and 74-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30,56-61 and 74-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-30, 56-61 and 74-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al. (6,096,582) in view of Mitani et al. (6,392,277).

Regarding claims 1-3, 5, 7-9, 13-14, 16, 18-19, 23, 25, 27 and 77-79, Inoue et al. teach in figure 2 and related text a transistor comprised of a channel region, said transistor comprising:

a bulk silicon substrate 1 and a silicon active layer 2, 3, 4;

an isolation structure 82'' (see figure 17A) formed in said active layer, said isolation structure defining an area;

a buried oxide layer 5, 6, 7 formed between said bulk silicon substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate,

a first section 6 positioned between two second sections 5, 7, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section 6 being less than said thickness of said second sections 5, 7; and

said active layer being formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer.

Inoue et al. do not teach a doped back gate region positioned at least partially in said bulk substrate under said multiple thickness buried oxide layer, wherein said doped back gate region extending under/beneath a source region and a drain region of the semiconductor device.

Mitani et al. teach in figure 8 and related text a doped back gate region 24A positioned at least partially in said bulk substrate 20 under said buried oxide layer 20B, wherein said doped back gate region extending under/beneath a source region and a drain region of the semiconductor device Qn.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a doped back gate region positioned at least partially in said bulk substrate under said multiple thickness buried oxide layer, wherein said doped back gate region extending under/beneath a source region and a drain region of the semiconductor device of Inoue et al.'s device in order to enhance the performance of the device when reducing the size of the device.

Regarding claims 10-11, 20-21, and 28-29, Inoue et al. teach in figure 2 and related text a transistor comprised of a gate electrode 8 and wherein said first section being substantially aligned with said gate electrode.

Regarding claims 4, 15 and 24, Inoue et al. teach in figure 2 and related text substantially the entire claimed structure, as applied to claims 1, 13 and 23 above, except using the device in at least one of a microprocessor, a memory device and a logic device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use Inoue et al.'s device in at least one of a microprocessor, a memory device and a logic device, in order to use the device in an application which requires at least one of a microprocessor, a memory device and a logic device.

Regarding claims 6, 12, 17, 22, 26 and 30, Inoue et al. teach in figure 2 and related text substantially the entire claimed structure, as applied to claims 1, 13 and 23 above, except stating that said first section has a thickness ranging from approximately 30-50 nm, said second sections have a thickness ranging from approximately 120-180 nm, and said active layer has a thickness ranging from approximately 5-30 nm.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a first section having a thickness ranging from approximately 30-50 nm, second sections having a thickness ranging from approximately 120-180 nm, and an active layer having a thickness ranging from approximately 5-30 nm, in Inoue et al.'s device in order to adjust and optimize the device electrical characteristics, which depend on the thicknesses of the buried oxide layer and the thickness of the active layer.

Regarding claims 56-64 and 74-76, Inoue et al. teach in figure 2 and related text a transistor comprised of a channel region, said transistor comprising:

a bulk silicon substrate 1 and an active layer 2, 3, 4, said active layer 2, 4 comprising a channel region being doped with a first type of dopant material;

a buried oxide layer 5, 6, 7 formed between said bulk silicon substrate and said active layer, said buried oxide layer comprising a substantially planar upper surface that contacts said active layer and a non-planar lower surface that contacts said bulk substrate, a first section positioned between two second sections, said first section having a thickness and each of said second sections having a thickness, said thickness of said first section being less than said thickness of said second sections;

said active layer formed above said buried oxide layer, said transistor being formed in said active layer above said buried oxide layer, at least a portion of said channel region being positioned above said first section of said buried oxide layer.

Inoue et al. do not teach a doped back gate region positioned at least partially in said bulk substrate under said buried oxide layer, wherein said doped back gate region being a doped region that is doped with a dopant material that is of the same type as that of said channel region.

Mitani et al. teach in figure 8 and related text a doped back gate region 24A positioned at least partially on said bulk substrate 20 under said buried oxide layer 20B, wherein said doped back gate region being a p-type doped region which is the dopant material that is of the same type as that of said channel region of semiconductor device Qn.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form a back gate region doped with the same conductivity type as that of the channel region and positioned at least partially on said bulk substrate under said buried oxide layer of Inoue et al.'s device in order to enhance the performance of the device when reducing the size of the device.

Response to Arguments

Applicant's arguments with respect to claims 1-30, 56-61 and 74-79 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference B is cited as being related to doped back gate in SOI devices.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

O.N.
6/4/2008

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